

SGM51652H4/SGM51652H8

16-Bit, 500kSPS, 4- and 8-Channel, Single Supply, SAR ADCs with Bipolar Input Ranges

GENERAL DESCRIPTION

The SGM51652H4 and SGM51652H8 are 4-channel and 8-channel, high-precision successive approximation (SAR) analog-to-digital converter (ADC).

These ADCs are powered by a single unipolar 5V, supports true bipolar $\pm 10.24V$, $\pm 5.12V$, and $\pm 2.56V$ inputs, as well as unipolar input ranges of 0V to 10.24V and 0V to 5.12V. The input range is configured by software.

These chips provides over-voltage protection at input, it's up to $\pm 20V$.

These chips have an on-chip high accuracy and low drift 10ppm reference.

The input impedance of these chips is $\geq 1M\Omega$ and it's dependent of input range selection.

The digital interface is compatible to the traditional SPI protocol.

FEATURES

- 16 Bits ADC
- Programmable Input Ranges:
 - ♦ Bipolar Ranges: $\pm 10.24V$, $\pm 5.12V$, and $\pm 2.56V$
 - ♦ Unipolar Ranges: 0V to 10.24V and 0V to 5.12V
- Supply Voltage Ranges:
 - ♦ Analog Supply: 5V
 - ♦ I/O Supply: 1.65V to 5V
- On-Chip Reference: 4.096V
- Differential Nonlinearity (DNL): $\pm 0.65LSB$
- Integral Nonlinearity (INL):
 - ♦ $\pm 1.1LSB$ for All Bipolar Ranges
 - ♦ $\pm 0.5LSB$ for All Unipolar Ranges
- Signal-to-Noise Ratio (SNR): 91dB
- Total Harmonic Distortion (THD): -102dB
- Alarm Features
- Daisy-Chain Operation
- -40°C to +125°C Operating Temperature Range
- Available in a Green TSSOP-38 Package

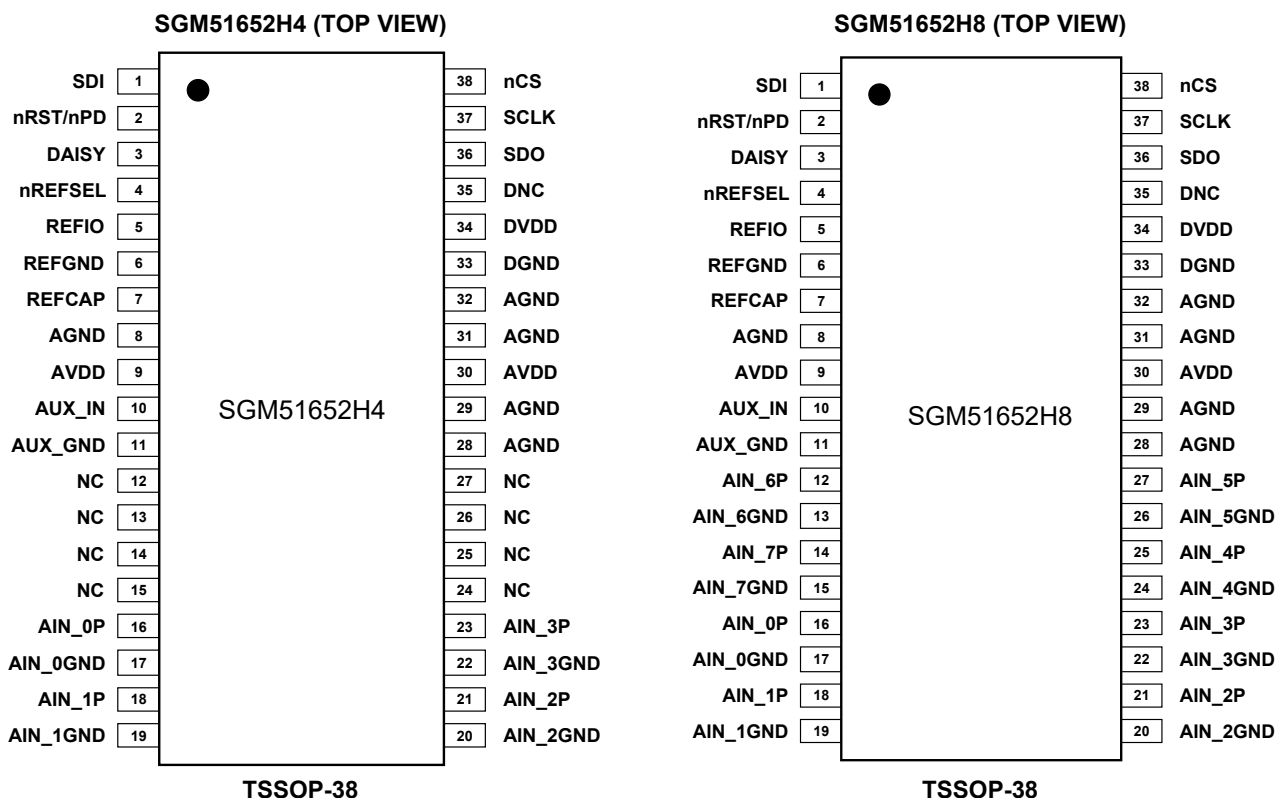
APPLICATIONS

PLC Analog Input Modules
Power Automation
Factory Automation
Protection Relays

SGM51652H4 SGM51652H8

16-Bit, 500kSPS, 4- and 8-Channel, Single Supply, SAR ADCs with Bipolar Input Ranges

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME		TYPE ⁽¹⁾	FUNCTION
	SGM51652H4	SGM51652H8		
1	SDI		DI	Serial Data Input.
2	nRST/nPD		DI	Dual-Function Pin: Reset/Power-Down the Device. Active low.
3	DAISY		DI	Chain the Serial Data Input in Daisy-Chain Mode.
4	nREFSEL		DI	Active Low. When it's enable, the Internal Reference is on.
5	REFIO		AIO	Internal Reference Output and External Reference Input Pin.
6	REFGND		P	Reference Ground Pin.
7	REFCAP		AO	ADC Reference Decoupling Capacitor Pin.
8	AGND		P	Analog Ground.
9	AVDD		P	Analog Power Supply.
10	AUX_IN		AI	Positive Auxiliary Input Pin.
11	AUX_GND		AI	Negative Auxiliary Input Pin.

SGM51652H4
SGM51652H8**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges****PIN DESCRIPTION (continued)**

PIN	NAME		TYPE ⁽¹⁾	FUNCTION
	SGM51652H4	SGM51652H8		
12	NC	AIN_6P	AI	Channel 6 Positive Analog Input.
13	NC	AIN_6GND	AI	Channel 6 Negative Analog Input.
14	NC	AIN_7P	AI	Channel 7 Positive Analog Input.
15	NC	AIN_7GND	AI	Channel 7 Negative Analog Input.
16	AIN_0P		AI	Channel 0 Positive Analog Input.
17	AIN_0GND		AI	Channel 0 Negative Analog Input.
18	AIN_1P		AI	Channel 1 Positive Analog Input.
19	AIN_1GND		AI	Channel 1 Negative Analog Input.
20	AIN_2GND		AI	Channel 2 Negative Analog Input.
21	AIN_2P		AI	Channel 2 Positive Analog Input.
22	AIN_3GND		AI	Channel 3 Negative Analog Input.
23	AIN_3P		AI	Channel 3 Positive Analog Input.
24	NC	AIN_4GND	AI	Channel 4 Negative Analog Input.
25	NC	AIN_4P	AI	Channel 4 Positive Analog Input.
26	NC	AIN_5GND	AI	Channel 5 Negative Analog Input.
27	NC	AIN_5P	AI	Channel 5 Positive Analog Input.
28, 29, 32	AGND		P	Analog Ground.
30	AVDD		P	Analog Power Supply.
31	AGND		P	Analog Ground.
33	DGND		P	Digital Ground.
34	DVDD		P	Digital Power Supply.
35	DNC		Do Not Connect	Do Not Connect This Pin. Keep it floating.
36	SDO		DO	Serial Data Output.
37	SCLK		DI	Serial Clock Input.
38	nCS		DI	Chip-Select Input Pin. Active low.

NOTE: 1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power Supply.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

ELECTRICAL CHARACTERISTICS

(AVDD = 5V, DVDD = 3V, VREF = 4.096V (internal), and fSAMPLE = 500kSPS, Full = -40°C to +125°C, typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Inputs						
Full-Scale Input Span ⁽¹⁾ (AIN_nP to AIN_nGND)		Input range = $\pm 2.5 \times V_{REF}$	$-2.5 \times V_{REF}$		$2.5 \times V_{REF}$	V
		Input range = $\pm 1.25 \times V_{REF}$	$-1.25 \times V_{REF}$		$1.25 \times V_{REF}$	
		Input range = $\pm 0.625 \times V_{REF}$	$-0.625 \times V_{REF}$		$0.625 \times V_{REF}$	
		Input range = $2.5 \times V_{REF}$	0		$2.5 \times V_{REF}$	
		Input range = $1.25 \times V_{REF}$	0		$1.25 \times V_{REF}$	
Operating Input Range, Positive Input (AIN_nP)		Input range = $\pm 2.5 \times V_{REF}$	$-2.5 \times V_{REF}$		$2.5 \times V_{REF}$	V
		Input range = $\pm 1.25 \times V_{REF}$	$-1.25 \times V_{REF}$		$1.25 \times V_{REF}$	
		Input range = $\pm 0.625 \times V_{REF}$	$-0.625 \times V_{REF}$		$0.625 \times V_{REF}$	
		Input range = $2.5 \times V_{REF}$	0		$2.5 \times V_{REF}$	
		Input range = $1.25 \times V_{REF}$	0		$1.25 \times V_{REF}$	
Operating Input Range, Negative Input (AIN_nGND)		All input ranges	-0.1	0	0.1	V
Input Impedance	Z _I	At TA = +25°C, all input ranges	0.85	1	1.15	MΩ
Input Impedance Drift		All input ranges		7	25	ppm/°C
Input Leakage Current	I _{kg(in)}	With voltage at AIN_nP pin = V _{IN} , input range = $\pm 2.5 \times V_{REF}$		$\frac{V_{IN} - 2.25}{R_{IN}}$		μA
		With voltage at AIN_nP pin = V _{IN} , input range = $\pm 1.25 \times V_{REF}$		$\frac{V_{IN} - 2.00}{R_{IN}}$		μA
		With voltage at AIN_nP pin = V _{IN} , input range = $\pm 0.625 \times V_{REF}$		$\frac{V_{IN} - 1.60}{R_{IN}}$		μA
		With voltage at AIN_nP pin = V _{IN} , input range = $2.5 \times V_{REF}$		$\frac{V_{IN} - 2.50}{R_{IN}}$		μA
		With voltage at AIN_nP pin = V _{IN} , input range = $1.25 \times V_{REF}$		$\frac{V_{IN} - 2.50}{R_{IN}}$		μA
Input Over-Voltage Protection						
Over-Voltage Protection Voltage	V _{OVP}	AVDD = 5V or offers low impedance < 30kΩ, all input ranges	-20		20	V
		AVDD = floating with impedance > 30kΩ, all input ranges	-11		11	V

NOTE:

1. Ideal input span, does not include gain or offset error.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3V, VREF = 4.096V (internal), and fSAMPLE = 500kSPS, Full = -40°C to +125°C, typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Performance						
Resolution			16			Bits
No Missing Codes	NMC		16			Bits
Differential Nonlinearity	DNL		-0.99	±0.5	1.5	LSB ⁽²⁾
Integral Nonlinearity ⁽³⁾	INL		-2	±0.75	2	LSB
Gain Error	EG	At TA = +25°C, all input ranges		±0.02	±0.05	%FSR ⁽⁴⁾
Gain Error Matching (Channel-to-Channel)		At TA = +25°C, all input ranges		±0.02	±0.05	%FSR
Gain Error Temperature Drift		All input ranges		±1	±4	ppm/°C
Offset Error	EO	At TA = +25°C, input range = ±2.5 × VREF		±0.5	±0.75	mV
		At TA = +25°C, input range = ±1.25 × VREF		±0.5	±1	
		At TA = +25°C, input range = ±0.625 × VREF		±0.5	±1.5	
		At TA = +25°C, input range = 0 to 2.5 × VREF		±0.5	±2	
		At TA = +25°C, input range = 0 to 1.25 × VREF		±0.5	±2	
Offset Error Matching (Channel-to-Channel)		At TA = +25°C, input range = ±2.5 × VREF		±0.5	±0.75	mV
		At TA = +25°C, input range = ±1.25 × VREF		±0.5	±1	
		At TA = +25°C, input range = ±0.625 × VREF		±0.5	±1.5	
		At TA = +25°C, input range = 0 to 2.5 × VREF		±0.5	±2	
		At TA = +25°C, input range = 0 to 1.25 × VREF		±0.5	±2	
Offset Error Temperature Drift		All input ranges		±1	±3	ppm/°C
Sampling Dynamics						
Conversion Time	tCONV				850	ns
Acquisition Time	tACQ		1150			ns
Maximum Throughput Rate without Latency	fs				500	kSPS

NOTES:

- LSB = least significant bit.
- This parameter is the endpoint INL, not best fit INL.
- FSR = full-scale range.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3V, VREF = 4.096V (internal), and fSAMPLE = 500kSPS, Full = -40°C to +125°C, typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Characteristics						
Signal-to-Noise Ratio (VIN - 0.5dBFS at 1kHz)	SNR	Input range = ±2.5 × VREF	90	92		dB
		Input range = ±1.25 × VREF	89	91		
		Input range = ±0.625 × VREF	87.5	89		
		Input range = 2.5 × VREF	88.5	90.5		
		Input range = 1.25 × VREF	87.5	89		
Total Harmonic Distortion ⁽⁵⁾ (VIN - 0.5dBFS at 1kHz)	THD	All input ranges		-102		dB
Signal-to-Noise Ratio (VIN - 0.5dBFS at 1kHz)	SINAD	Input range = ±2.5 × VREF	89	91.5		dB
		Input range = ±1.25 × VREF	88.5	91		
		Input range = ±0.625 × VREF	87	89		
		Input range = 2.5 × VREF	87.5	90.5		
		Input range = 1.25 × VREF	87	89		
Spurious-Free Dynamic Range (VIN - 0.5dBFS at 1kHz)	SFDR	All input ranges		103		dB
Crosstalk Isolation ⁽⁶⁾		Aggressor channel input is overdriven to 2 × maximum input voltage		110		dB
Crosstalk Memory ⁽⁷⁾		Aggressor channel input is overdriven to 2 × maximum input voltage		90		dB
Small-Signal Bandwidth	-3dB	BW _{-3dB}	At TA = +25°C, all input ranges		15	kHz
	-0.1dB	BW _{-0.1dB}	At TA = +25°C, all input ranges		2.5	kHz
Auxiliary Channel						
Resolution			16			Bits
AUX_IN Voltage Range	VAUX_IN	AUX_IN - AUX_GND	0		VREF	V
Operating Input Range		AUX_IN	0		VREF	V
		AUX_GND		0		
Input Capacitance	C1	During sampling		75		pF
		During conversion		5		
Input Leakage Current	I _{lkg(in)}			100		nA
Differential Nonlinearity	DNL		-0.99	±0.6	1.5	LSB
Integral Nonlinearity	INL		-4	±1.5	4	LSB
Gain Error	EG(AUX)	At TA = +25°C		±0.02	±0.2	% FSR
Offset Error	EO(AUX)	At TA = +25°C	-10		10	mV
Signal-to-Noise Ratio	SNR	VAUX_IN = -0.5dBFS at 1kHz	87	89		dB
Total Harmonic Distortion ⁽⁵⁾	THD	VAUX_IN = -0.5dBFS at 1kHz		-102		dB
Signal-to-Noise + Distortion	SINAD	VAUX_IN = -0.5dBFS at 1kHz	86	88.5		dB
Spurious-Free Dynamic Range	SFDR	VAUX_IN = -0.5dBFS at 1kHz		103		dB

NOTES:

5. Accumulated the first nine harmonics.

6. Any off-channel with 10 kHz, Full-scale sinusoidal input to channel being sampled with DC input.

7. From previously sampled to channel with 10kHz, Full-scale sinusoidal input to channel being sampled with DC input.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), and f_{SAMPLE} = 500kSPS, Full = -40°C to +125°C, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Internal Reference Output							
Voltage on REFIO Pin (Configured as Output) ⁽⁸⁾	V _{REFIO_INT}	At T _A = +25°C	4.095	4.096	4.097	V	
Internal Reference Temperature Drift				6	10	ppm/°C	
Decoupling Capacitor on REFIO	C _{OUT_REFIO}		10	22		μF	
Reference voltage to ADC (on REFCAP pin)	V _{REFCAP}	At T _A = +25°C	4.095	4.096	4.097	V	
Reference Buffer Output Impedance				0.5	1	Ω	
Reference Buffer Temperature Drift				0.6	1.5	ppm/°C	
Decoupling Capacitor on REFCAP	C _{OUT_REFCAP}		10	22		μF	
Turn-On Time		C _{OUT_REFCAP} = 22μF, C _{OUT_REFIO} = 22μF		15		ms	
External Reference Input							
External Reference Voltage on REFIO (Configured as Input)	V _{REFIO_EXT}		4.046	4.096	4.146	V	
Power-Supply Requirements							
Analog Power-Supply Voltage	AVDD	Analog supply	4.75	5	5.25	V	
Digital Power-Supply Voltage	DVDD	Digital supply range	1.65	3.3	AVDD	V	
		Digital supply range for specified performance	2.7	3.3	5.25	V	
Analog Supply Current	Dynamic, AVDD	I _{AVDD_DYN}	AVDD = 5V, f _S = maximum and internal reference	SGM51652H8	13	16	mA
				SGM51652H4	8.5	11.5	mA
	Static	I _{AVDD_STC}	AVDD = 5V, device not converting and internal reference	SGM51652H8	10	12	mA
				SGM51652H4	5.5	8.5	mA
Standby	I _{STDBY}	At AVDD = 5V, device in STDBY mode and internal reference		3	4.5	mA	
Power-Down	I _{PWR_DN}	At AVDD = 5V, device in PWR_DN		3	20	μA	
Digital Supply Current	I _{DVDD_DYN}	At DVDD = 3.3V, output = 0000h		0.5		mA	
Digital Inputs (CMOS)							
Digital Input Logic Levels DVDD > 2.1V	V _{IH}		0.7 × DVDD		DVDD + 0.3	V	
	V _{IL}		-0.3		0.3 × DVDD	V	
Digital Input Logic Levels DVDD ≤ 2.1V	V _{IH}		0.8 × DVDD		DVDD + 0.3	V	
	V _{IL}		-0.3		0.2 × DVDD	V	
Input Leakage Current				100		nA	
Input Pin Capacitance				5		pF	
Digital Outputs (CMOS)							
Digital Output Logic Levels	V _{OH}	I _O = 500μA source	0.8 × DVDD		DVDD	V	
	V _{OL}	I _O = 500μA sink	0		0.2 × DVDD	V	
Floating State Leakage Current		Only for SDO		1		μA	
Internal Pin Capacitance				5		pF	

NOTE:

8. Does not consider soldering shift effects.

SGM51652H4
SGM51652H8**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges****TIMING REQUIREMENTS: SERIAL INTERFACE**

(AVDD = 5V, DVDD = 3V, V_{REF} = 4.096V (internal), SDO load = 20pF, and f_{SAMPLE} = 500kSPS, Full = -40°C to +125°C, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timing Specifications						
Sampling Frequency (f _{CLK} = max)	f _S				500	kSPS
ADC Cycle Time Period (f _{CLK} = max)	t _S		2			μs
Serial Clock Frequency (f _S = max)	f _{SCLK}				66.6	MHz
Serial Clock Time Period (f _S = max)	t _{SCLK}		1/f _{SCLK}			ns
Conversion Time	t _{CONV}				850	ns
Delay Time: nCS Falling to Data Enable	t _{DZ_CSDO}				10	ns
Delay Time: Last SCLK Falling to nCS Rising	t _{D_CKCS}		10			ns
Delay Time: nCS Rising to SDO Going to 3-State	t _{DZ_CSDO}		10			ns
Timing Requirements						
Acquisition Time	t _{ACQ}		1150			ns
Clock High Time	t _{PH_CK}		0.4		0.6	t _{SCLK}
Clock Low Time	t _{PL_CK}		0.4		0.6	t _{SCLK}
nCS High Time	t _{PH_CS}		30			ns
Setup Time: nCS Falling to SCLK Falling	t _{SU_CSCK}		30			ns
Hold Time: SCLK Falling to (Previous) Data Valid on SDO	t _{HT_CKDO}		5			ns
Setup Time: SDO Data Valid to SCLK Falling	t _{SU_DOCK}		5			ns
Setup Time: SDI Data Valid to SCLK Falling	t _{SU_DICK}		5			ns
Hold Time: SCLK Falling to (Previous) Data Valid on SDI	t _{HT_CKDI}		5			ns
Setup Time: DAISY Data Valid to SCLK Falling	t _{SU_DSCK}		5			ns
Hold Time: SCLK Falling to (Previous) Data Valid on DAISY	t _{HT_CKDSY}		5			ns

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS

R/W: Read/Write bit(s)

R: Read only bit(s)

The internal registers are divided into two categories: command registers and program registers.

Command Register Description

Table 1. Command Register Map

Register	MSB Byte								LSB Byte	Command (Hex)	Operation in Next Frame
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power-Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset Program Registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence with Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch 0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch 1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected
Manual Ch 2 Selection (MAN_Ch 2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch 3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual Ch 4 Selection (MAN_Ch 4) ⁽¹⁾	1	1	0	1	0	0	0	0	0000 0000	D000h	Channel 4 input is selected
Manual Ch 5 Selection (MAN_Ch 5) ⁽¹⁾	1	1	0	1	0	1	0	0	0000 0000	D400h	Channel 5 input is selected
Manual Ch 6 Selection (MAN_Ch 6) ⁽¹⁾	1	1	0	1	1	0	0	0	0000 0000	D800h	Channel 6 input is selected
Manual Ch 7 Selection (MAN_Ch 7) ⁽¹⁾	1	1	0	1	1	1	0	0	0000 0000	DC00h	Channel 7 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

NOTE:

1. The bits or registers are not included in the SGM5152H4.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS (continued)

Program Register Description

Table 2. Program Register Map

Register	Register Address Bits[15:9]	Default Value ⁽¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Auto Scan Sequencing Control										
AUTO_SEQ_EN	01h	FFh	CH7_EN ⁽²⁾	CH6_EN ⁽²⁾	CH5_EN ⁽²⁾	CH4_EN ⁽²⁾	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Channel Power-Down	02h	00h	CH7_PD ⁽²⁾	CH6_PD ⁽²⁾	CH5_PD ⁽²⁾	CH4_PD ⁽²⁾	CH3_PD	CH2_PD	CH1_PD	CH0_PD
Device Features Selection Control										
Feature Select	03h	00h	DEV[1:0]		0	0	0	SDO [2:0]		
Range Select Registers										
Channel 0 Input Range	05h	00h	0	0	0	0	Range Select Channel 0 [3:0]			
Channel 1 Input Range	06h	00h	0	0	0	0	Range Select Channel 1 [3:0]			
Channel 2 Input Range	07h	00h	0	0	0	0	Range Select Channel 2 [3:0]			
Channel 3 Input Range	08h	00h	0	0	0	0	Range Select Channel 3 [3:0]			
Channel 4 Input Range ⁽²⁾	09h	00h	0	0	0	0	Range Select Channel 4 [3:0]			
Channel 5 Input Range ⁽²⁾	0Ah	00h	0	0	0	0	Range Select Channel 5 [3:0]			
Channel 6 Input Range ⁽²⁾	0Bh	00h	0	0	0	0	Range Select Channel 6 [3:0]			
Channel 7 Input Range ⁽²⁾	0Ch	00h	0	0	0	0	Range Select Channel 7 [3:0]			
Command Read Back (Read-Only)										
Command Read Back	3Fh	00h	COMMAND_WORD [7:0]							
Input Floating Detection and Status										
INPUT_FLOATING_DETECTION_EN	0Dh	00h	CH7_EN ⁽²⁾	CH6_EN ⁽²⁾	CH5_EN ⁽²⁾	CH4_EN ⁽²⁾	CH3_EN	CH2_EN	CH1_EN	CH0_EN
INPUT_FLOATING_DETECTION_STATUS	0Eh	00h	CH7_FT ⁽²⁾	CH6_FT ⁽²⁾	CH5_FT ⁽²⁾	CH4_FT ⁽²⁾	CH3_FT	CH2_FT	CH1_FT	CH0_FT

NOTES:

1. All registers are reset to the default values at power-on or a reset operation.
2. The bits or registers are not included in the SGM5152H4.

SGM51652H4
SGM51652H8**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges****REGISTER MAPS (continued)****Auto-Scan Sequencing Control Registers**

Table 3. AUTO_SEQ_EN Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7]	CH7_EN ⁽¹⁾	Channel 7 Enable 0 = Channel 7 is not selected for sequencing in AUTO_RST mode 1 = Channel 7 is selected for sequencing in AUTO_RST mode		R/W	1h
D[6]	CH6_EN ⁽¹⁾	Channel 6 Enable 0 = Channel 6 is not selected for sequencing in AUTO_RST mode 1 = Channel 6 is selected for sequencing in AUTO_RST mode		R/W	1h
D[5]	CH5_EN ⁽¹⁾	Channel 5 Enable 0 = Channel 5 is not selected for sequencing in AUTO_RST mode 1 = Channel 5 is selected for sequencing in AUTO_RST mode		R/W	1h
D[4]	CH4_EN ⁽¹⁾	Channel 4 Enable 0 = Channel 4 is not selected for sequencing in AUTO_RST mode 1 = Channel 4 is selected for sequencing in AUTO_RST mode		R/W	1h
D[3]	CH3_EN	Channel 3 Enable 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode		R/W	1h
D[2]	CH2_EN	Channel 2 Enable 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode		R/W	1h
D[1]	CH1_EN	Channel 1 Enable 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode		R/W	1h
D[0]	CH0_EN	Channel 0 Enable 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode		R/W	1h

NOTE:

1. The bits or registers are not included in the SGM5152H4.

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
 SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS (continued)

Channel Power-Down Register (Address = 02h)

Table 4. Channel Power-Down Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7]	CH7_PD ⁽¹⁾	Channel 7 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[6]	CH6_PD ⁽¹⁾	Channel 6 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[5]	CH5_PD ⁽¹⁾	Channel 5 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[4]	CH4_PD ⁽¹⁾	Channel 4 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[3]	CH3_PD	Channel 3 Power-Down 0 = channel is on. 1 = channel is power down.		R/W	0h
D[2]	CH2_PD	Channel 2 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[1]	CH1_PD	Channel 1 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h
D[0]	CH0_PD	Channel 0 Power-Down 0 = channel is on 1 = channel is power down		R/W	0h

NOTE:

1. The bits or registers are not included in the SGM5152H4.

**SGM51652H4
SGM51652H8**

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS (continued)

Device Feature Selection Control Register (Address = 03h)

Table 5. Feature Select Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7:6]	DEV[1:0]	Device ID Bits 00 = ID for device 0 in daisy-chain mode 01 = ID for device 1 in daisy-chain mode 10 = ID for device 2 in daisy-chain mode 11 = ID for device 3 in daisy-chain mode		R/W	0h
D[5]	0	Must always be set to 0		R	0h
D[4]	0	Must always be set to 0		R	0h
D[3]	0	Must always be set to 0		R	0h
D[2:0]	SDO[2:0]	SDO Data Format Bits	Refer to Table 6	R/W	0h

Table 6. SDO Data Format

SDO Format SDO[2:0]	Beginning of The Output Bit Stream	Output Format			
		BITS [24:9]	BITS [8:5]	BITS [4:3]	BITS [2:0]
000	16 th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	SDO pulled low		
001	16 th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address ⁽¹⁾	SDO pulled low	
010	16 th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address ⁽¹⁾	Device address ⁽¹⁾	SDO pulled low
011	16 th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address ⁽¹⁾	Device address ⁽¹⁾	Input range ⁽¹⁾

NOTE:

1. Table 7 lists the bit descriptions for these channel addresses, device addresses, and input range.

Table 7. SDO Data Bit Details

BITS	DESCRIPTION
D[24:9]	16 bits of conversion result for the channel represented in MSB-first format.
D[8:5]	Four Bits of Channel Address 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 (valid only for the SGM51652H8) 0101 = Channel 5 (valid only for the SGM51652H8) 0110 = Channel 6 (valid only for the SGM51652H8) 0111 = Channel 7 (valid only for the SGM51652H8)
D[4:3]	Two bits of device address (mainly useful in daisy-chain mode).
D[2:0]	Three LSB bits of input voltage range (refer to the Range Select Registers section).

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS (continued)

Range Select Registers (Addresses 05h - 0Ch)

Table 8. Channel n Input Range Registers Details

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7:4]	0	Must always be set to 0		R	0h
D[3:0]	Range_CHn[3:0]	Input range selection bits for channel n (n = 0 to 3 for the SGM51652H4 and n = 0 to 7 for the SGM51652H8) 0000 = Input range is set to $\pm 2.5 \times V_{REF}$ 0001 = Input range is set to $\pm 1.25 \times V_{REF}$ 0010 = Input range is set to $\pm 0.625 \times V_{REF}$ 0101 = Input range is set to 0 to $2.5 \times V_{REF}$ 0110 = Input range is set to 0 to $1.25 \times V_{REF}$		R/W	0h

Command Read-Back Register (Address = 3Fh)

Table 9. Command Read-Back Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7:0]	COMMAND_WORD[15:8]	Command executed in previous data frame		R	0h

SGM51652H4
SGM51652H8

**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

REGISTER MAPS (continued)

Input Floating Detection and Status (Address = 0Dh - 0Eh)

Table 10. INPUT_FLOATING_DETECTION_EN Register Details (Address = 0Dh)

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7]	CH7_EN ⁽¹⁾	Channel 7 Enable 0 = Channel 7 is disabled in FLOATING_DETECTION mode 1 = Channel 7 is enabled in FLOATING_DETECTION mode		R/W	0h
D[6]	CH6_EN ⁽¹⁾	Channel 6 Enable 0 = Channel 6 is disabled in FLOATING_DETECTION mode 1 = Channel 6 is enabled in FLOATING_DETECTION mode		R/W	0h
D[5]	CH5_EN ⁽¹⁾	Channel 5 Enable 0 = Channel 5 is disabled in FLOATING_DETECTION mode 1 = Channel 5 is enabled in FLOATING_DETECTION mode		R/W	0h
D[4]	CH4_EN ⁽¹⁾	Channel 4 Enable 0 = Channel 4 is disabled in FLOATING_DETECTION mode 1 = Channel 4 is enabled in FLOATING_DETECTION mode		R/W	0h
D[3]	CH3_EN	Channel 3 Enable 0 = Channel 3 is disabled in FLOATING_DETECTION mode 1 = Channel 3 is enabled in FLOATING_DETECTION mode		R/W	0h
D[2]	CH2_EN	Channel 2 Enable 0 = Channel 2 is disabled in FLOATING_DETECTION mode 1 = Channel 2 is enabled in FLOATING_DETECTION mode		R/W	0h
D[1]	CH1_EN	Channel 1 Enable 0 = Channel 1 is disabled in FLOATING_DETECTION mode 1 = Channel 1 is enabled in FLOATING_DETECTION mode		R/W	0h
D[0]	CH0_EN	Channel 0 Enable 0 = Channel 0 is disabled in FLOATING_DETECTION mode 1 = Channel 0 is enabled in FLOATING_DETECTION mode		R/W	0h

NOTE:

1. The bits or registers are not included in the SGM5152H4.

Table 11. INPUT_FLOATING_DETECTION_STATUS Register Details (Address = 0Eh)

BITS	BIT NAME	DESCRIPTION	COMMENT	TYPE	RESET
D[7]	CH7_FT ⁽¹⁾	Channel 7 FLOATINT_STATUS 0 = Channel 7 is not in FLOATING status 1 = Channel 7 is in FLOATING status		R/W	0h
D[6]	CH6_FT ⁽¹⁾	Channel 6 FLOATINT_STATUS 0 = Channel 6 is not in FLOATING status 1 = Channel 6 is in FLOATING status		R/W	0h
D[5]	CH5_FT ⁽¹⁾	Channel 5 FLOATINT_STATUS 0 = Channel 5 is not in FLOATING status 1 = Channel 5 is in FLOATING status		R/W	0h
D[4]	CH4_FT ⁽¹⁾	Channel 4 FLOATINT_STATUS 0 = Channel 4 is not in FLOATING status 1 = Channel 4 is in FLOATING status		R/W	0h
D[3]	CH3_FT	Channel 3 FLOATINT_STATUS 0 = Channel 3 is not in FLOATING status 1 = Channel 3 is in FLOATING status		R/W	0h
D[2]	CH2_FT	Channel 2 FLOATINT_STATUS 0 = Channel 2 is not in FLOATING status 1 = Channel 2 is in FLOATING status		R/W	0h
D[1]	CH1_FT	Channel 1 FLOATINT_STATUS 0 = Channel 1 is not in FLOATING status 1 = Channel 1 is in FLOATING status		R/W	0h
D[0]	CH0_FT	Channel 0 FLOATINT_STATUS 0 = Channel 0 is not in FLOATING status 1 = Channel 0 is in FLOATING status		R/W	0h

NOTE:

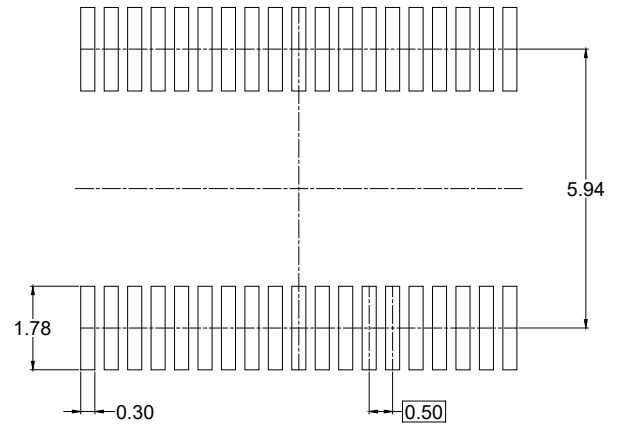
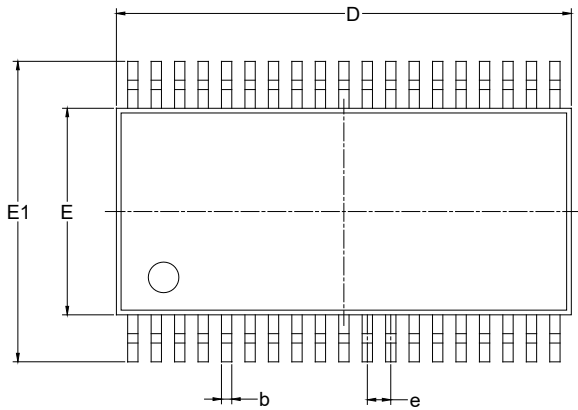
1. The bits or registers are not included in the SGM5152H4.

SGM51652H4
SGM51652H8

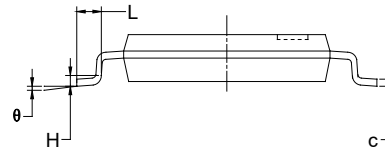
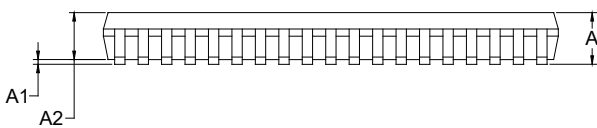
**16-Bit, 500kSPS, 4- and 8-Channel, Single Supply,
SAR ADCs with Bipolar Input Ranges**

PACKAGE OUTLINE DIMENSIONS

TSSOP-38



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.500 BSC		0.020 BSC	
H	0.250 TYP		0.010 TYP	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.