5.5V-100V Vin, 1.8A Peak Current Limit, High Efficiency Asynchronous Step-down DCDC Converter

FEATURES

- Wide Input Range: 5.5V-100V
- Maximum Output Voltage: 30V
- 1A Continuous Output Current
- 1.8A Peak Current Limit when V_{IN}<60V
- Integrated 970mΩ High-Side Power MOSFET
- 49uA Quiescent Current
- 1.2V Feedback Reference Voltage
- 3.5ms Internal Soft-start Time
- Fixed Switching Frequency at 390KHz
- COT Control Mode with Integrated Loop Compensation
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Cycle-by-Cycle Current Limiting
- Over-Voltage Protection
- Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- 48V Distributed Power Delivery Bus
- Battery Management System (e-Bike, Scooter)
- Motor Drives, Drones

DESCRIPTION

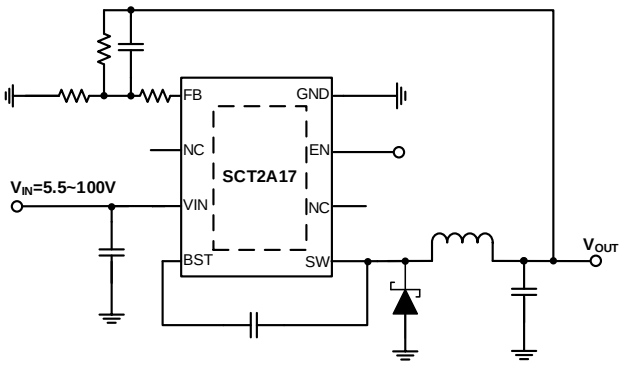
The SCT2A17 is an asynchronous buck converter with wide input voltage ranging from 5.5V to 100V which accommodates a variety of step-down applications, making it ideal for automotive, industry, and lighting applications. The SCT2A17 integrates an 970mΩ high-side MOSFET and has 1.8A peak output current limit when V_{IN}<60V to support high peak current application.

The SCT2A17, adopting the constant-on time (COT) mode control with integrated loop compensation greatly simplifies the converter off-chip configuration.

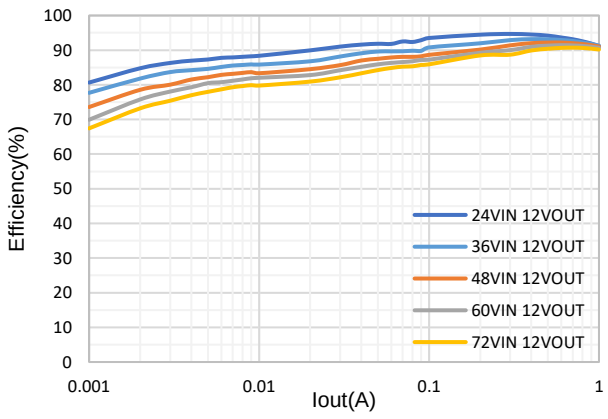
The SCT2A17 features Pulse Frequency Modulation (PFM) mode at light load with typical 49uA low quiescent current, which enables the converter to achieve the high-power efficiency during light-load or no-load conditions.

The SCT2A17 offers cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced ESOP-8 package.

TYPICAL APPLICATION



5.5V-100V, Asynchronous Buck Converter



Efficiency, Vout=12V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2A17STER	Tape & Reel	4000	2A17	8	ESOP-8

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	105	V
BST	-0.3	110	V
SW	-1	105	V
BST-SW	-0.3	5.5	V
EN (2)	-0.3	6.5	V
FB	-0.3	5.5	V
Operating junction temperature T_J (3)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) This parameter is a theoretical design value, and a Zener diode is installed inside the pin for protection.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

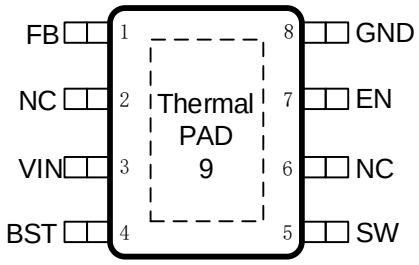


Figure 1. 8-Lead Plastic E-SOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
FB	1	Inverting input of the comparator. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1.2V typical.
NC	2	Not Connection.
VIN	3	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
BST	4	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
SW	5	Regulator switching output. Connect SW to an external power inductor
NC	6	Not Connection.
EN	7	Enable pin to the regulator with internal pull-up current source. Pull below 1.24V to disable the converter. Floating to enable the converter.
GND	8	Ground
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	5.5	100	V
V_{OUT}	Output voltage range	1.2	30	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	1	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	38.89	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.4	
Ψ_{JB}	Junction-to-board characterization parameter(1)	20.47	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	71.99	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	20.89	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A17 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A17. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		5.5		100	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising	4.55	5	5.45	V
		Hysteresis		420		mV
I_{SHDN}	Shutdown current from V_{IN} pin	EN=0, no load		4.3	8	uA
		Tj=-40°C~125°C			10	uA
I_Q	Quiescent current from V_{IN} pin	EN floating, no load, non- switching, BOOT-SW=5V	30	49	65	uA
		Tj=-40°C~125°C	20		80	uA
I_A	Active current from V_{IN} pin*	EN floating, no load, V_{OUT}=12V		68		uA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V	600	970	1700	mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.17	1.2	1.23	V
		Tj=-40°C~125°C	1.16		1.24	V
Enable and Soft-startup						
V_{EN_H}	Enable high threshold		1.2	1.24	1.3	V
V_{EN_Hys}	Enable threshold hysteresis			10		mV
I_{EN_L}	Enable pin pull-up current	EN=0V		0.37		uA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		2.07		μA
I_{EN_Hys}	Enable pin pull-up current hysteresis			1.7		uA
V_{EN_Clamp}	Enable pin clamp voltage	Force 100uA Current into EN pin		6.3		V
T_{ss}	Internal soft start time			3.5		ms
Switching Frequency Timing						
F_{SW}	Switching frequency		290	390	490	kHz
T_{OFF_MIN}	Minimum off time			250		ns
Current Limit and Over Current Protection						
I_{LIM}	HS MOSFET current limit	VIN＜60V	1.25	1.8	2.5	A
		VIN≥60V	0.95	1.5	2.2	A
T_hiccup	Hiccup mode off-time after activation			7		SS cycles
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		120		%
		V_{FB}/V_{REF} falling		115		%
V_{UVP}	Feedback under voltage with respect to reference voltage	V_{FB}/V_{REF} rising		45		%
		V_{FB}/V_{REF} falling		40		%
T_{SD}	Thermal shutdown threshold*	T_J rising		155		°C
		Hysteresis		13		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

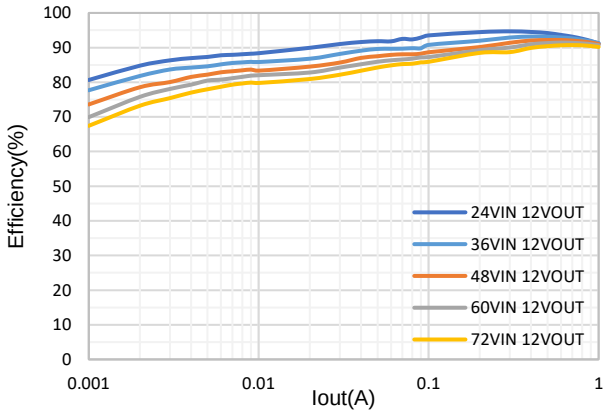


Figure 2. Efficiency vs Load Current, Vout=12V

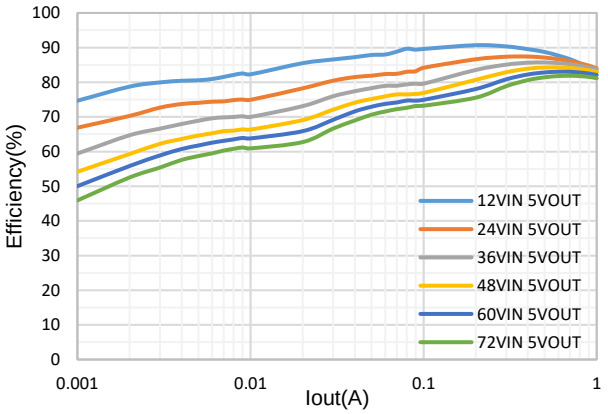


Figure 3. Efficiency vs Load Current, Vout=5V

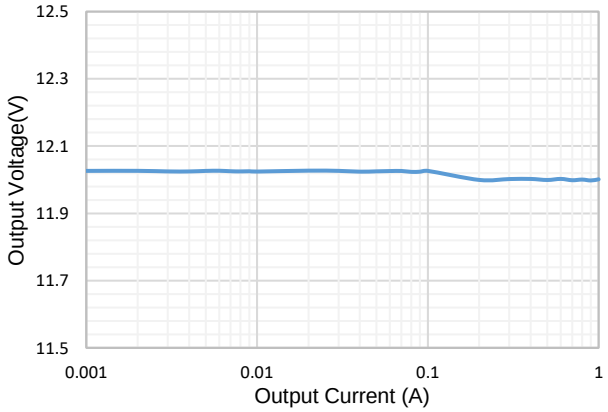


Figure 4. Load Regulation, Vin=48V, Vout=12V

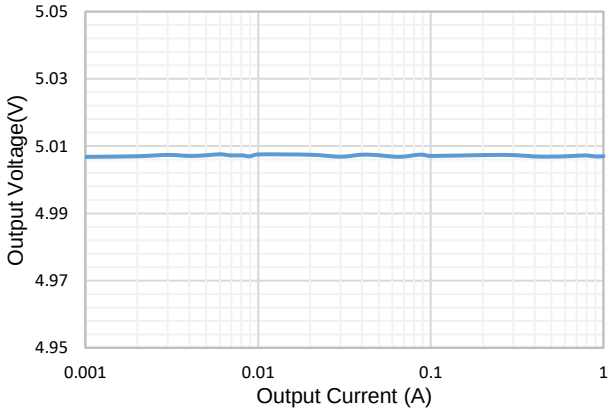


Figure 5. Load Regulation, Vin=24V, Vout=5V

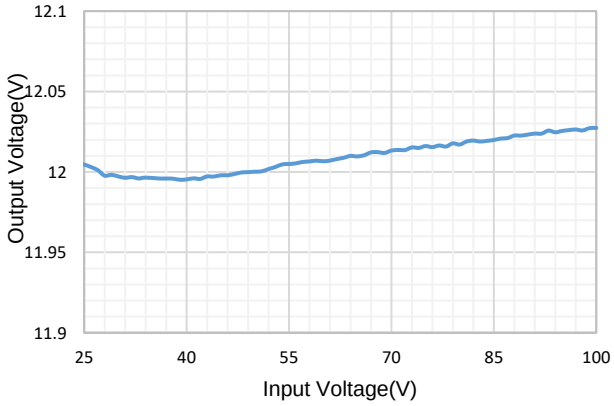


Figure 6. Line Regulation, Iout=1A

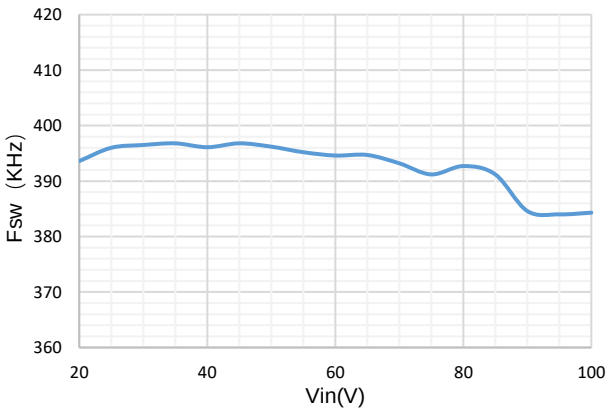


Figure 7. Switching Frequency vs Vin, Vout=12V

FUNCTIONAL BLOCK DIAGRAM

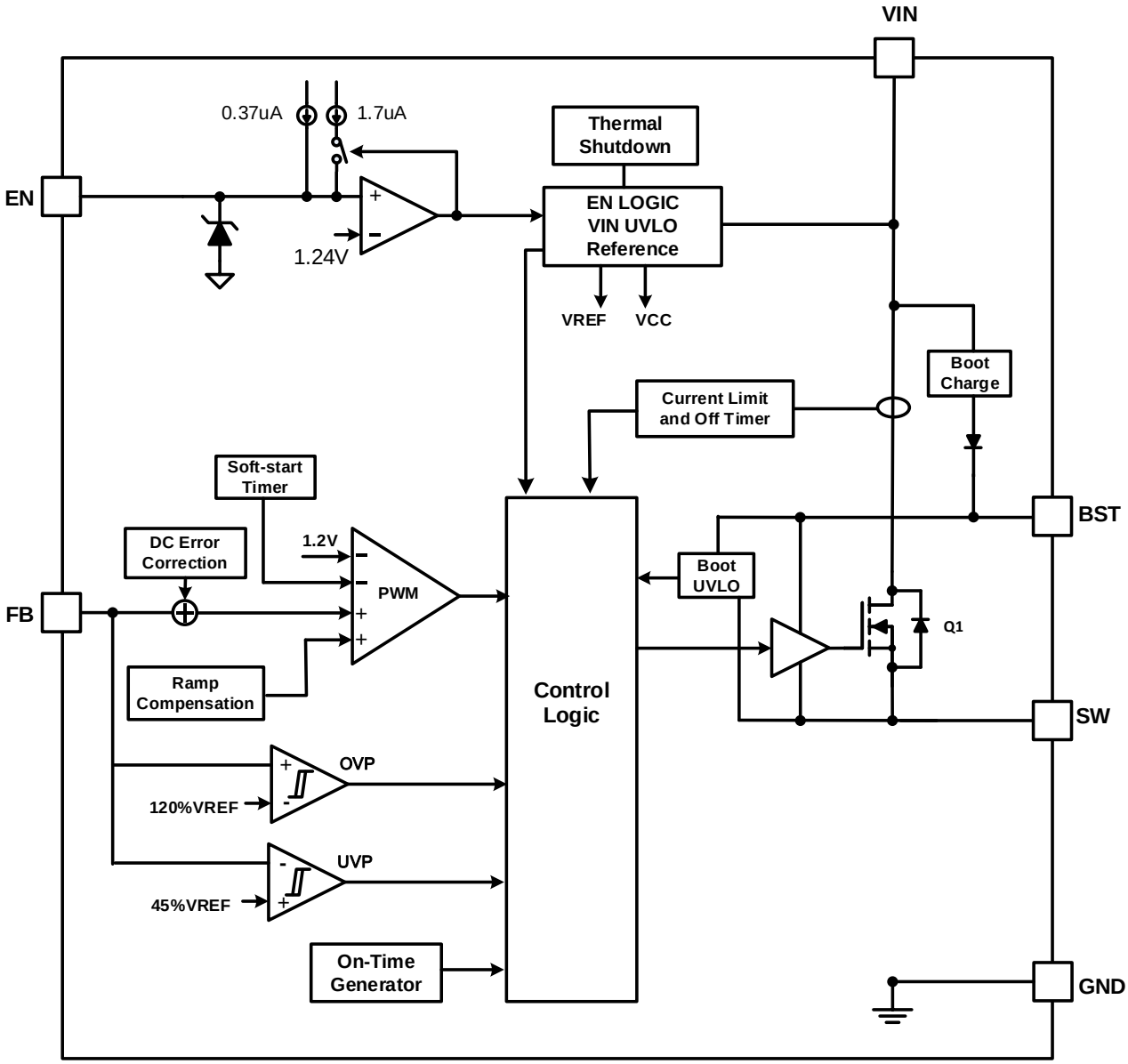


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2A17 is a 5.5V-100V input, 1.8A peak current limit when V_{IN}<60V, Step-down DCDC converter with built-in 970mΩ high-side power MOSFET. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier integrated improve the line and load regulation.

The SCT2A17 features an internal 3.5ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency is fixed at 390KHz. The device also supports monolithic startup with pre-biased output condition.

The SCT2A17 has a default input start-up voltage of 5V with 420mV hysteresis. The EN pin has a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin.

The SCT2A17 full protection features include the VIN input under-voltage lockout, the output over-voltage and under-voltage protection, over current protection with cycle-by-cycle current limit, output hard short protection and thermal shutdown protection.

Constant On-Time Mode Control

The SCT2A17 employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and output voltage. After the on-time, the high-side MOSFET (Q1) turns off. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreased below the VREF or SS, the Q1 turns on again after another dead time duration. This repeats on cycle-by-cycle.

The SCT2A17 works with an internal compensation, so customer could use the device easily. Feedforward cap C_f is necessary to provide flexibility for optimizing the loop stability and transient response.

Enable and Under Voltage Lockout Threshold

The SCT2A17 is enabled when the VIN pin voltage rises above 5V and the EN pin voltage exceeds the enable threshold of 1.24V. The device is disabled when the VIN pin voltage falls below 4.58V or when the EN pin voltage is below 1.23V. Internal pull up current source to EN pin allows the device enable when EN pin floats.

There is a Zener diode inside the EN pin. When the voltage of the EN pin is higher than 6.3V, the Zener diode conducts to clamp the voltage. To protect the Zener diode, the current flowing through it cannot exceed 200uA.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN\_H} * \frac{R3 + R4}{R4} \quad (1)$$

$$VIN\_hys = I2 * R3 \quad (2)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I_2=1.7uA

V_{EN_H}=1.24V

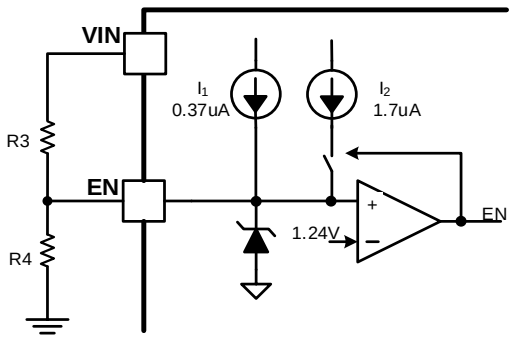


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2A17 regulates the internal reference voltage at 1.2V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2A17 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.2V reference voltage in 3.5ms. If the EN pin is pulled below 1.23V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off.

The UVLO of high-side MOSFET gate driver has rising threshold of 3.19V and hysteresis of 290mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.9V, BOOT UVLO occurs. The converter forces turning off high-side MOSFET to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

To maintain bootstrap capacitor voltage, please output at least 10mA load current when V_{IN}—V_{OUT} < 2V, at least 30mA load current when V_{IN}—V_{OUT} < 1V.

Over Current Limit, Hiccup Mode and Under Voltage Protection

The inductor current is monitored during high-side FET turn on. The SCT2A17 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current during unexpected overload or output hard short.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously (V_{UVP_F}), the converter stops switching. After remaining OFF for 7 SS cycles， the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make FB voltage lower than V_{UVP_R}, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

SCT2A17 also provide a HS current limit off timer for making the IC safer when trigger over current condition. Once trigger HS over current, the present on-time period is immediately terminated to avoid the inductor current run away. The length of off time is controlled by FB voltage and VIN voltage and could be calculated by the following Equation.

$$T_{off} = 1.5 * \left(\frac{V_{IN}}{20 * V_{FB} + 4.35}\right) us \quad (4)$$

Over Voltage Protection

The SCT2A17 implements the Over-Voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP

circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 120% of internal 1.2V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 115% of the 1.2V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2A17 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 155°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 142°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical application

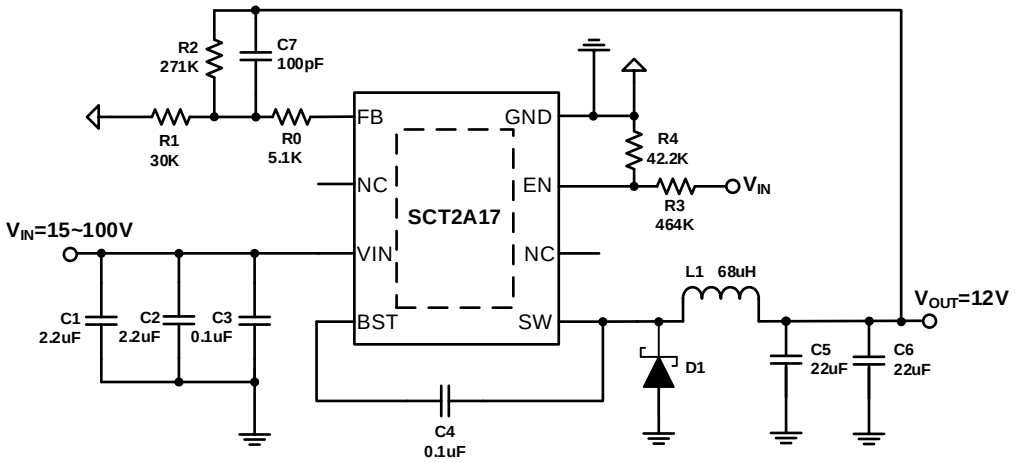


Figure 10. SCT2A17 Design Example, 12V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal, 15V to 100V
Output Voltage	12V
Maximum Output Current	1A
Switching Frequency	390 KHz
Output voltage ripple (peak to peak)	10mV
Transient Response 0.25A to 0.75A load step	ΔVout = 69mV

Output Voltage

The output voltage is set by an external resistor divider R_1 and R_2 in typical application schematic. Recommended R_1 resistance is 30KΩ. Use Equation 5 to calculate R_2.

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_1 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage of 1.2V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_2	R_1
5 V	95 KΩ	30 KΩ
12 V	271 KΩ	30 KΩ
24V	191 KΩ	10 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_3 from the input to EN pin and R_4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. When selecting resistors, it is important to consider that the current flowing through the Zener diode should not exceed 200uA.

For the example design, the supply should turn on and start switching once the input voltage increases above 15V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 14V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 464 kΩ and 42.2 kΩ of R_3 and R_4 resistors.

$$VIN_{rise} = V_{EN\_H} * \frac{R3 + R4}{R4} \quad (6)$$

$$VIN\_hys = I2 * R3 \quad (7)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I_2=1.7uA

V_{EN_H}=1.24V

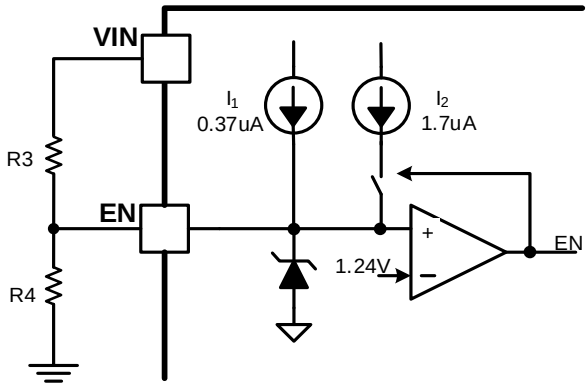


Figure 11. System UVLO by enable divide

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (8)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (9)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 10 and Equation 11.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (10)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (11)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 1.8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 1.8A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2A17 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The SCT2A17 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 100-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2A17.

For the example design, the SS310B Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the SS310B is 0.7 volts at 1A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 12 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The SS310B diode has a junction capacitance of 400 pF. Using Equation 12, the total loss in the diode at the maximum input voltage is 0.8W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN\_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN\_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_d)^2}{2} \quad (12)$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, two 2.2μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

Table 2 lists typical values of external components for some standard output voltages.

Table 2: Component List with Typical Output Voltage BOM list

Vout	L1	COUT	R2	R1	C7
5V	47uH	2*22uF	95K	30K	100pF
12V	68uH	2*22uF	271K	30K	100pF
24V	150uH	2*22uF	191k	10K	220pF

Application Waveforms

Vin=48V, Vout=12V, unless otherwise noted

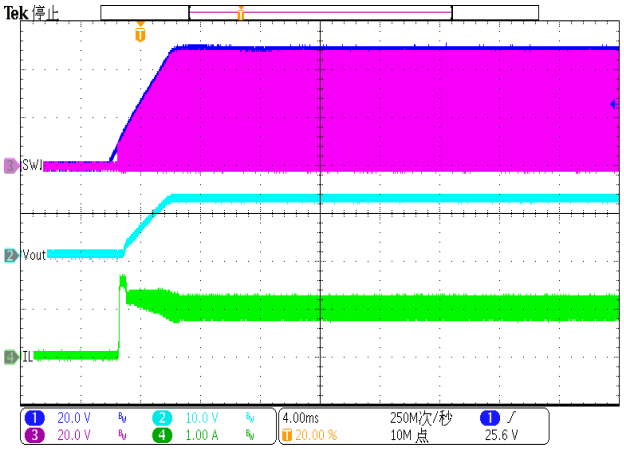


Figure 12. Power up (Iload=1A)

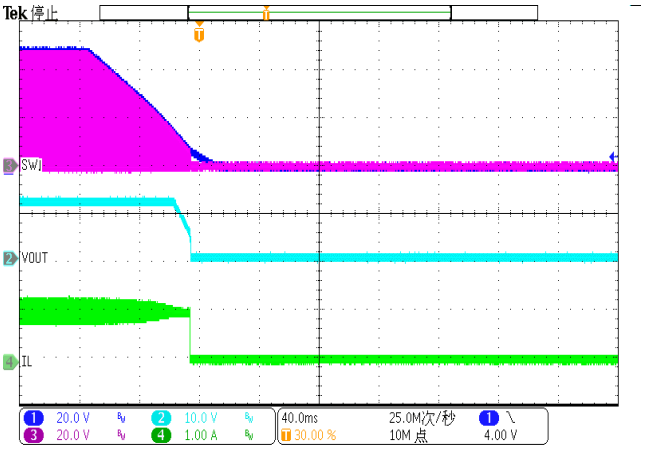


Figure 13. Power down (Iload=1A)

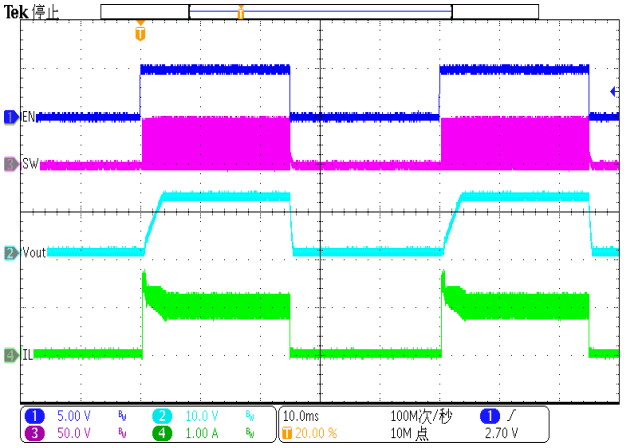


Figure 14. EN toggle (Iload=1A)

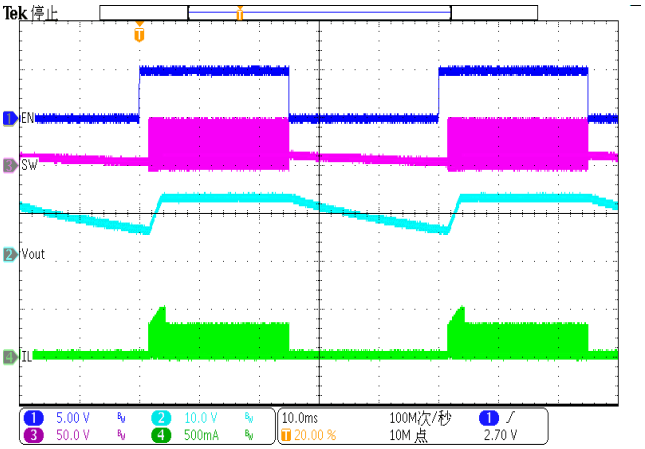


Figure 15. EN toggle (Iload=10mA)

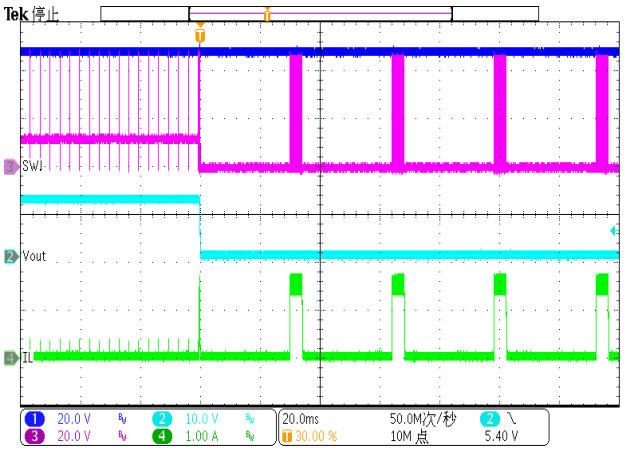


Figure 16. Over Current Protection

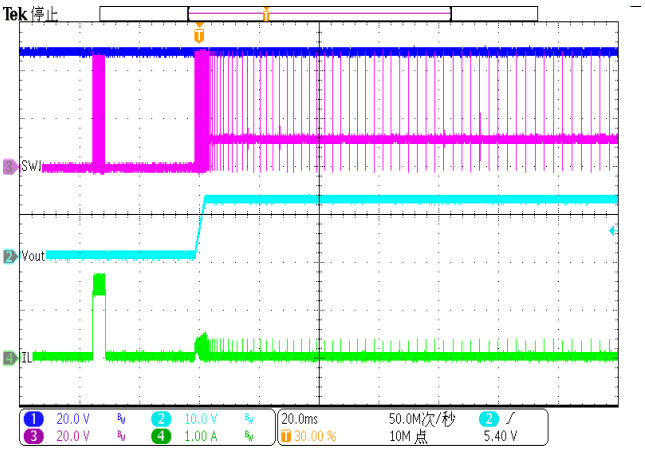


Figure 17. Over Current Release

Application Waveforms(Continued)

Vin=48V, Vout=12V, unless otherwise noted

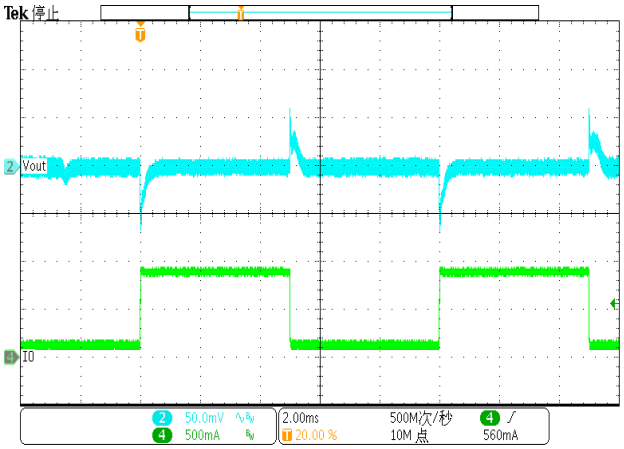


Figure 18. Load Transient (0.1A-0.9A, 1.6A/us)

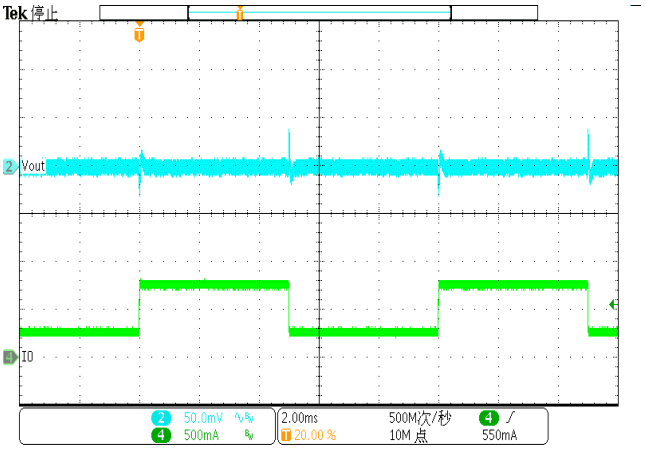


Figure 19. Load Transient (0.25A-0.75A, 1.6A/us)

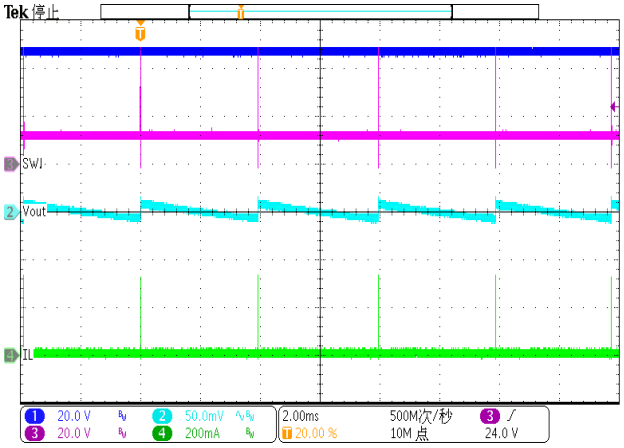


Figure 20. Output Ripple (Iload=0A)

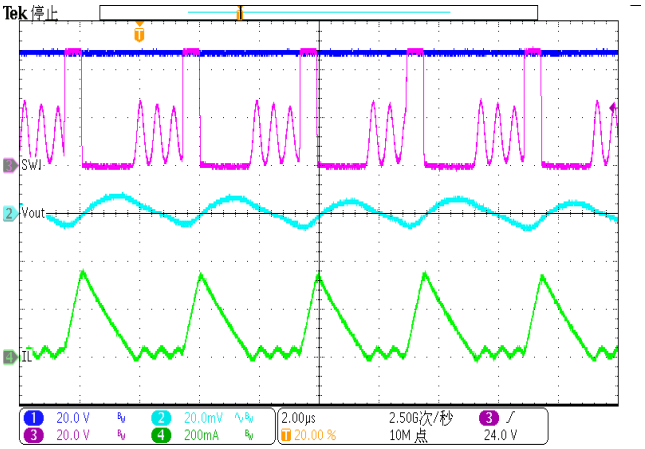


Figure 21. Output Ripple (Iload=0.1A)

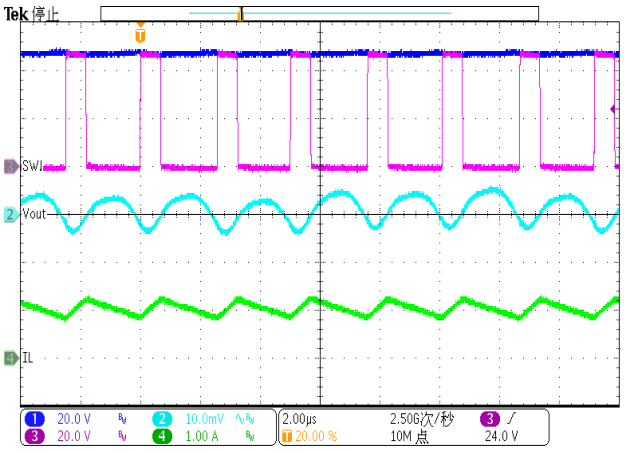


Figure 22. Output Ripple (Iload=1A)

Figure 23. Thermal, 48VIN, 12Vout,1A

Layout Guideline

Proper PCB layout is a critical for SCT2A17's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Route BST capacitor trace on the bottom layer to provide wide path for topside ground.

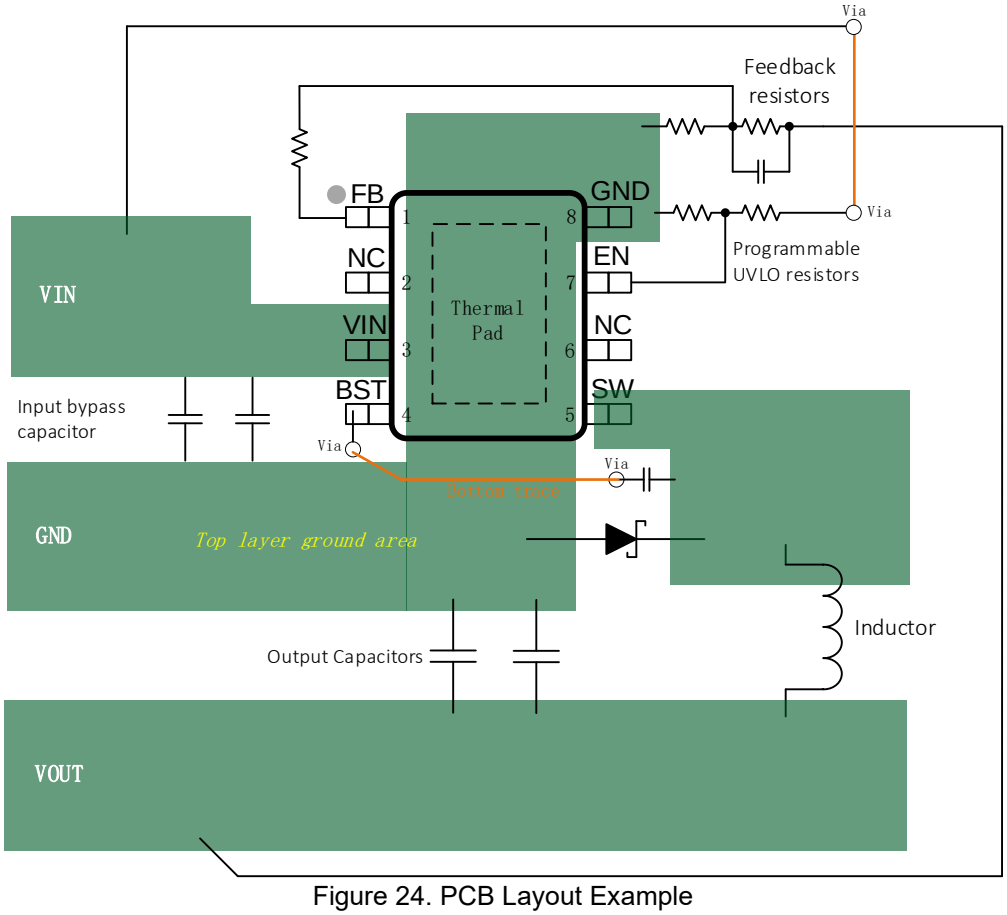
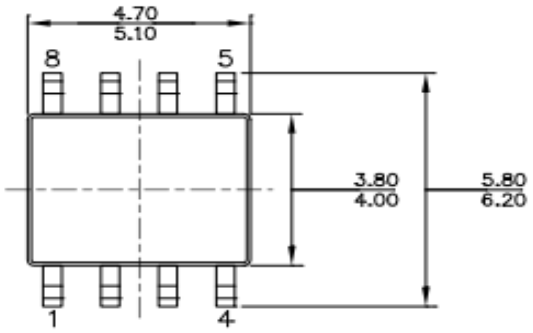


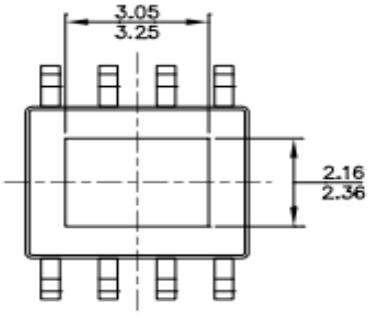
Figure 24. PCB Layout Example

PACKAGE INFORMATION

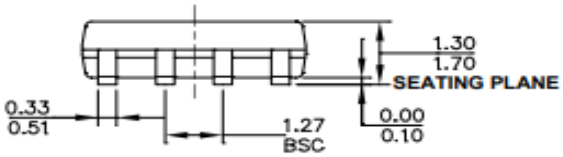
PACKAGE OUTLINE DRAWING FOR 8L SOP-EP
POD-0022 Revision 0.0



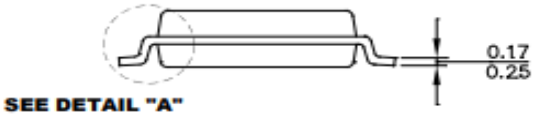
TOP VIEW



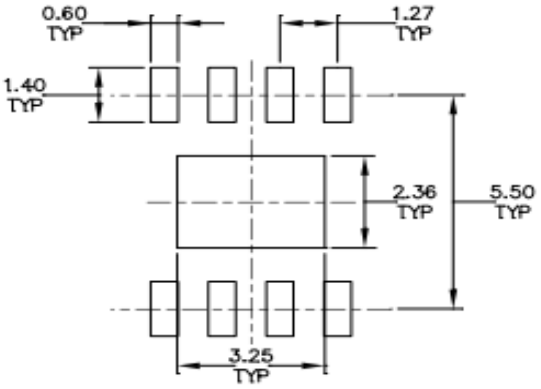
TOP VIEW



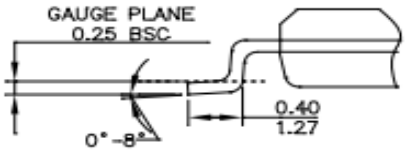
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

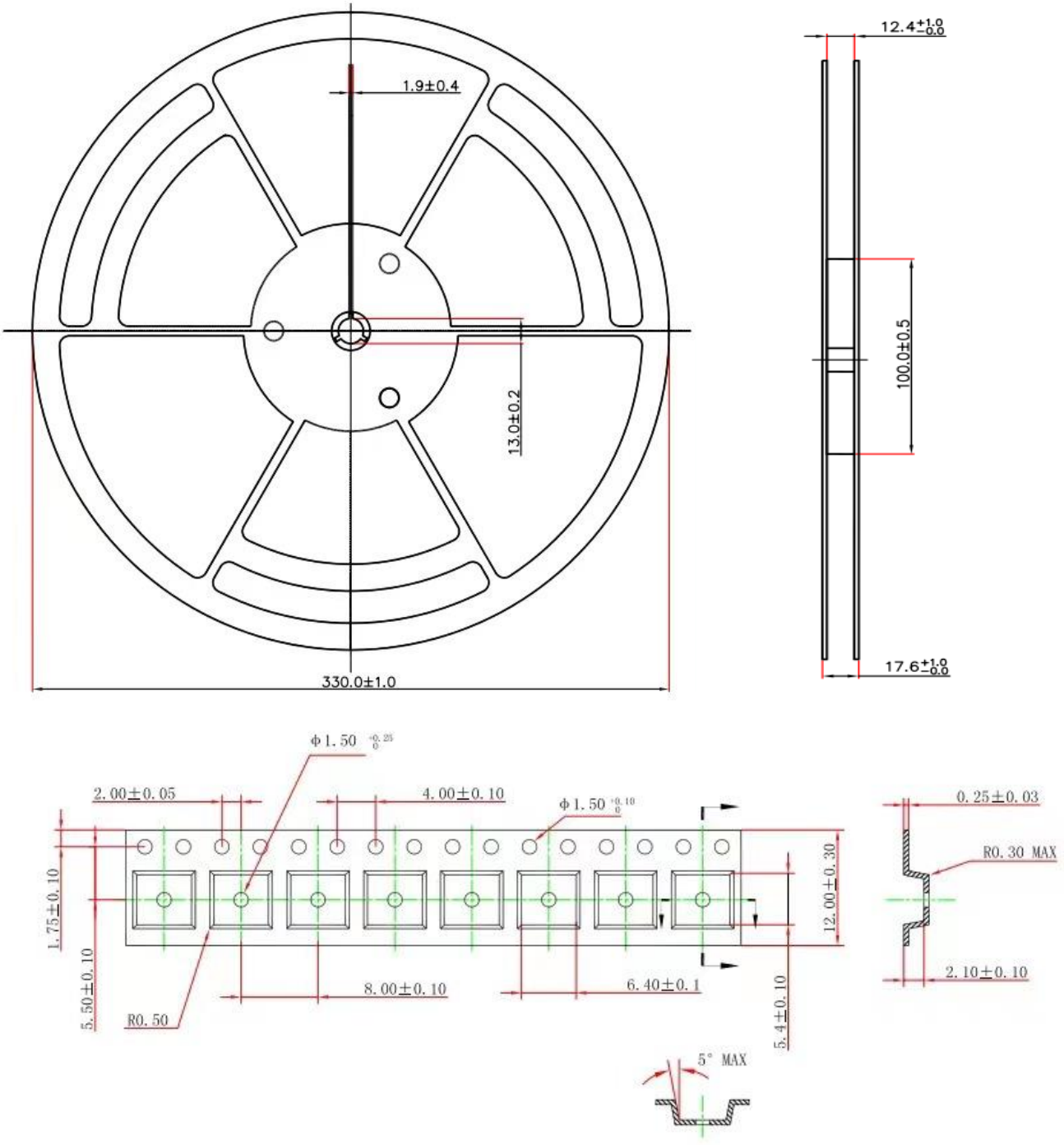


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



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